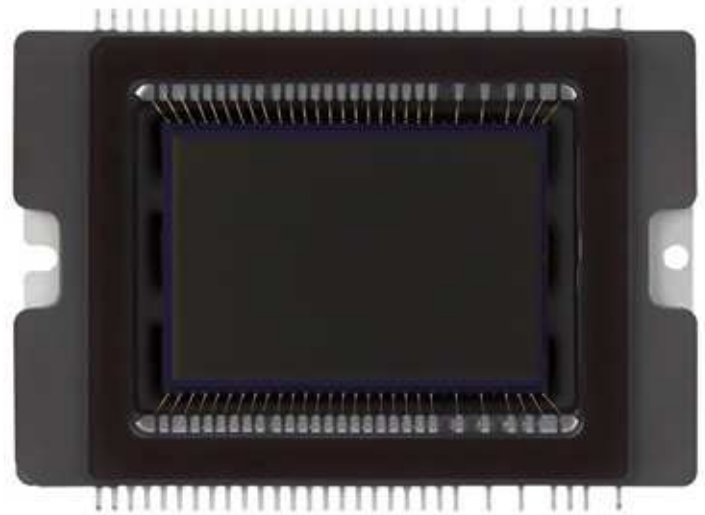


The module acquires data from CMOS sensor and controls its analogue inputs.

Hardware IP cores and image preprocessing IP cores are developed. Interface with host CPU was realized.



Specifications

FPGA-type	Xilinx Spartan3-250
Employed buses and memory interfaces	<ul style="list-style-type: none"> • EEPROM,SDRAM • JTAG,USB2.0
Developed IP Cores	<ul style="list-style-type: none"> • Scanning/buffering • Binning • IIC Interface • Synchronization • DAC controller • SDRAM controller • DMA controller
Design tools	ISE Xilinx, ChipScope Pro
Lead time	2 months