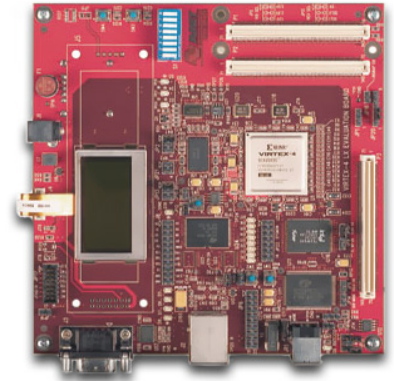


The controller is designed for two video-streams composition purposes: first stream is from CMOS sensor, the second is artificial computer-generated. «Frame-by-frame» editing algorithm is embedded with ability to generate the resulting output stream with a different video resolution and standard. Silica (AVNET) debugging boards, Texas Instruments 6416 DSK and user-defined video input daughterboard are implemented in the system.



High-speed Micron MT9M CMOS video-sensor with VGA resolution and a wide range of frame reading speed (15...90 frames per second) is used. Standard video-interfaces such as Component video, Composite video, S-video based on «front-end» interface chips from Analog Devices have been applied. The user-defined image-filters for mixing, correlation, edge detection SAD calculation and ROI extraction as well as the «host-target» applications for communication with the workstation have been developed. High-speed interfaces USB 2.0 and 2xEthernet 10/100 are used for connectivity purposes.

Specifications

FPGA-type	Xilinx Virtex4-FX12
DSP-type	Texas Instruments TMS320C6416T
Employed buses and FPGA memory interface	PLB, OPB, APU, OCM DDR, BRAM, NAND Flash
Employed buses and DSP memory interface	EMIF, EDMA, GPIO SDRAM, EEPROM
Employed connectivity interfaces	<ul style="list-style-type: none"> • Tri-MAC Ethernet 10/100 • USB 2.0 • UART
Developed IP cores	<ul style="list-style-type: none"> • Application-specific image processing filters • Flash memory controller • Bus controller IIC, SPI • FPGA to DSP bridge
Peculiarities	<ul style="list-style-type: none"> • Sensor`s system frequency - 30 MHz • Processor: PowerPC 405 -350 MHz • Operating system: MontaVista Linux, DSP\BIOS
Design tools	ISE Xilinx, EDK, Code Composer Studio 3.0, Chip Scope Pro, gcc, Cross Toolchain for PowerPC405
Lead time	9 months