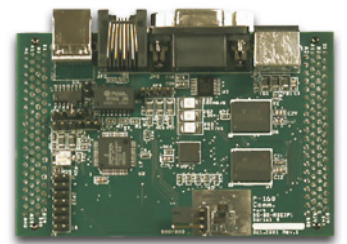
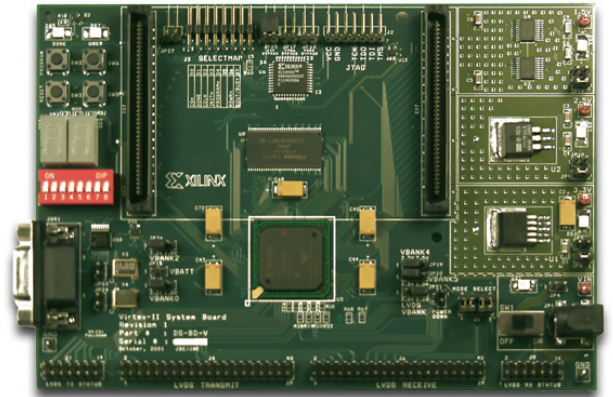


The controller is designed with ability to receipt, analyze and to distribute the user-defined UDP messages in Ethernet LAN. Two Memec (Avnet) debugging boards, user-defined daughterboard with six physical Ethernet PHY devices have been implemented in the present system.

The system contains two Microblaze processor cores which exchange data via BRAM and one more Picoblaze processor core as an interrupt controller. The bundled messages are simultaneously receiving by six Ethernet controllers and forwarding for subsequent frames preprocessing, post-processing and future analysis.

To ensure the above-mentioned processes, hardware IP cores, «target» applications and drivers for embedded ucLinux operating system was developed.



Specifications

| | |
|--------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FPGA-type | Xilinx VirtexII-1000 |
| Employed buses and memory interfaces | LMB, OPB, FSL SDRAM, Toshiba Flash |
| Employed connectivity interfaces | <ul style="list-style-type: none"> • Ethernet 10/100 • UART • JTAG |
| Developed IP cores | <ul style="list-style-type: none"> • Frame buffer/multiplexer • CRC checker and generator • Packet interpreter/composer • ARP\RARP\IP Look up tables • NAND Flash Controller |
| Peculiarities | <ul style="list-style-type: none"> • Processor Microblaze 66 MHz • Processor Picoblaze 66 MHz • ucLinux operating system |
| Design tools | ISE Xilinx, EDK, ChipScope Pro, gcc, Crosscompiler Toolchain Microblaze, Picoblaze assembler |
| Lead time | 5 months |